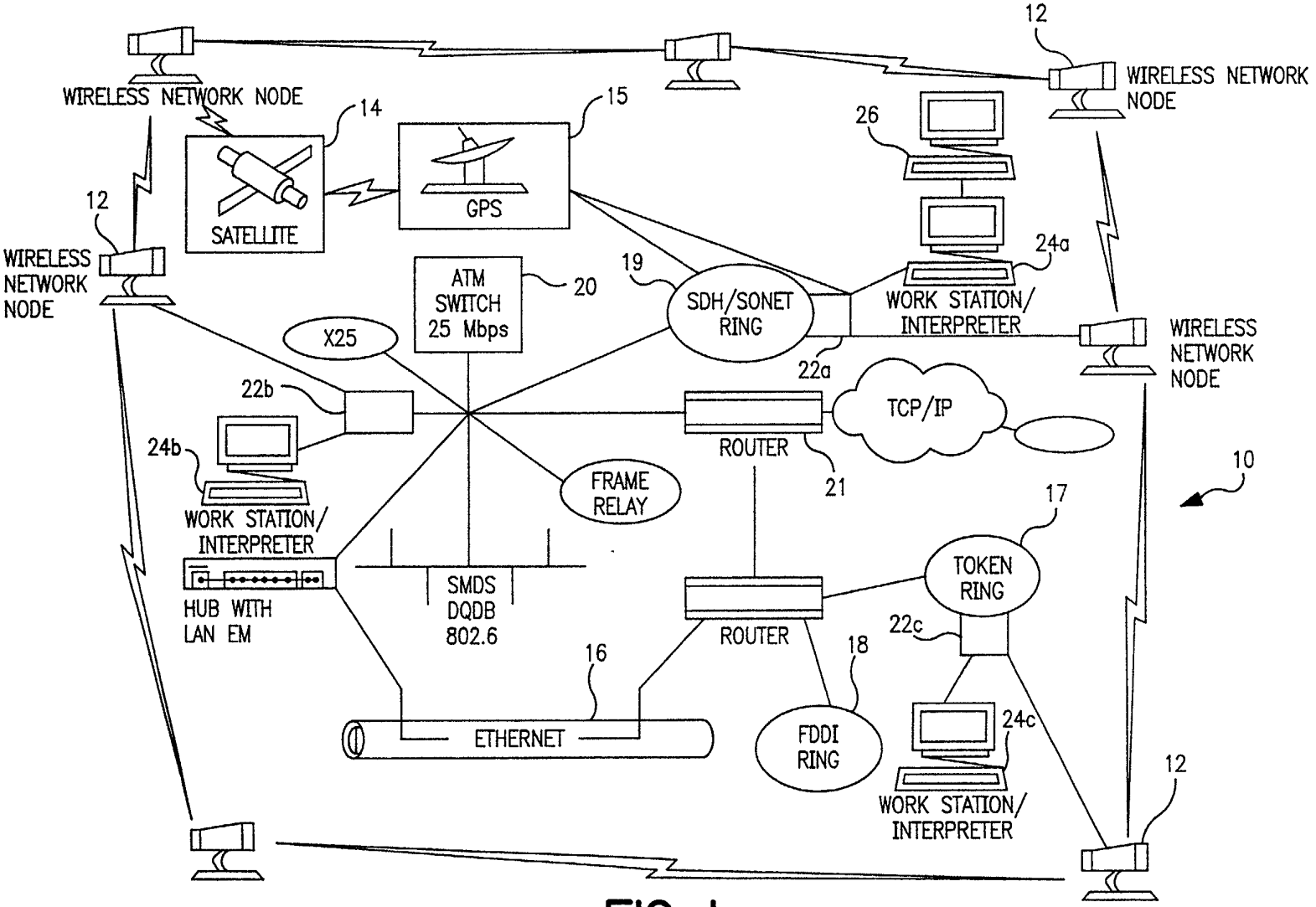

FIG. 1

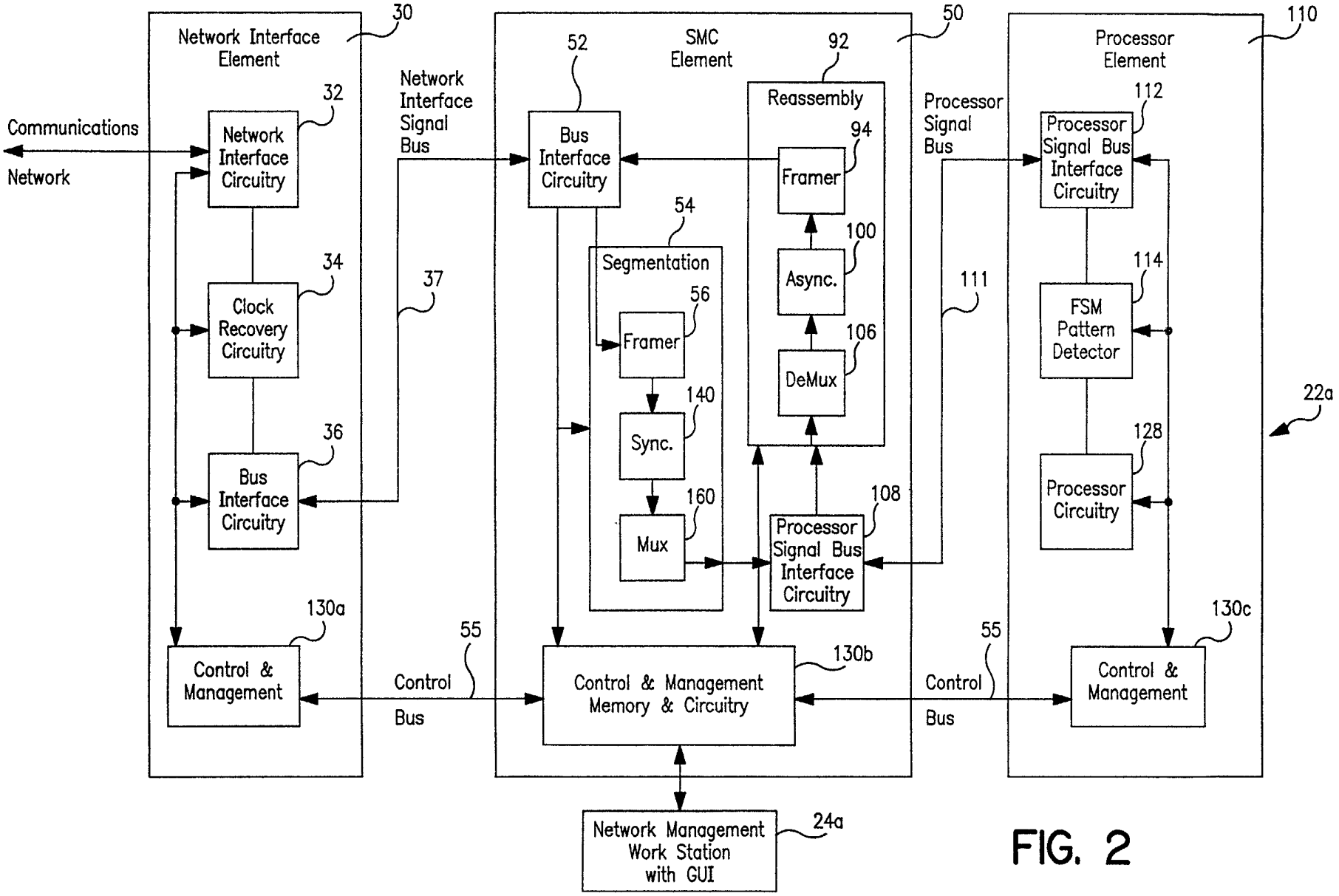
Network Interface Element
30
Communications Network
32
Network Interface Circuitry
34
Clock Recovery Circuitry
36
Bus Interface Circuitry
37
Network Interface Signal Bus
130a
Control & Management
55
Control Bus
SMC Element
50
52
Bus Interface Circuitry
54
Segmentation
56
Framer
140
Sync.
160
Mux
92
Reassembly
94
Framer
100
Async.
106
DeMux
108
Processor Signal Bus Interface Circuitry
130b
Control & Management Memory & Circuitry
Network Management Work Station with GUI
24a
Processor Signal Bus
111
Processor Element
110
112
Processor Signal Bus Interface Circuitry
114
FSM Pattern Detector
128
Processor Circuitry
130c
Control & Management
55
Control Bus
22a

FIG. 2

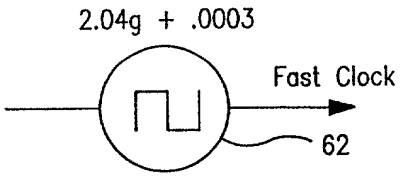
2.04g + .0003
Fast Clock
62

FIG. 3b

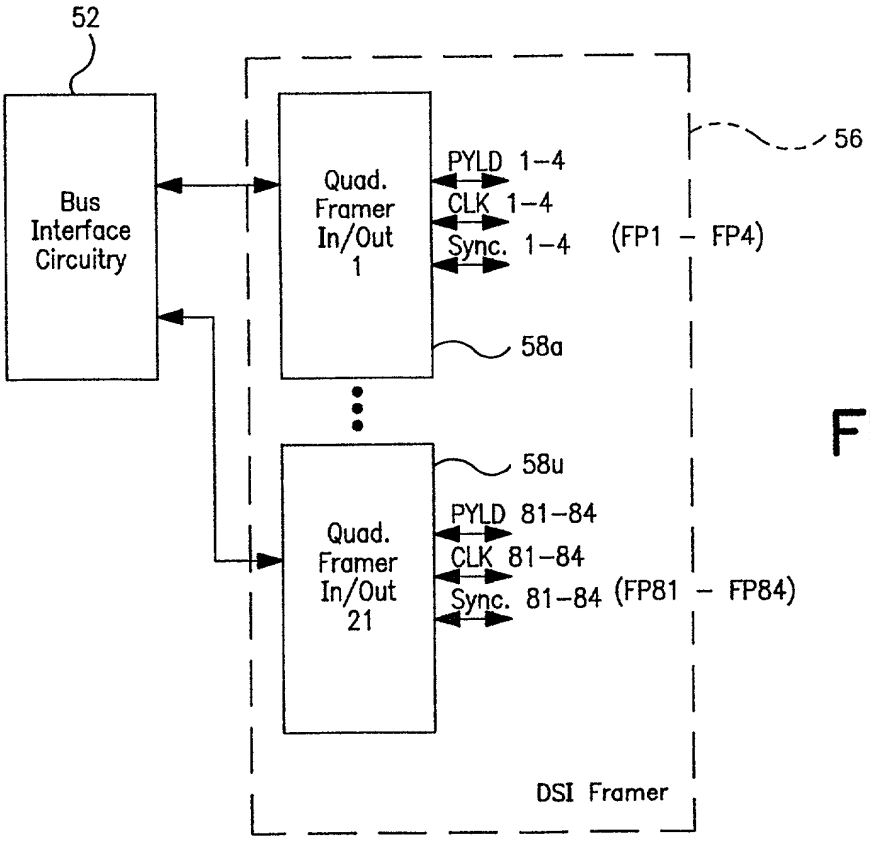
52
Bus Interface Circuitry
Quad. Framer In/Out 1
PYLD 1-4
CLK 1-4
Sync. 1-4
(FP1 - FP4)
56
58a
58u
Quad. Framer In/Out 21
PYLD 81-84
CLK 81-84
Sync. 81-84 (FP81 - FP84)
DSI Framer

FIG. 3a

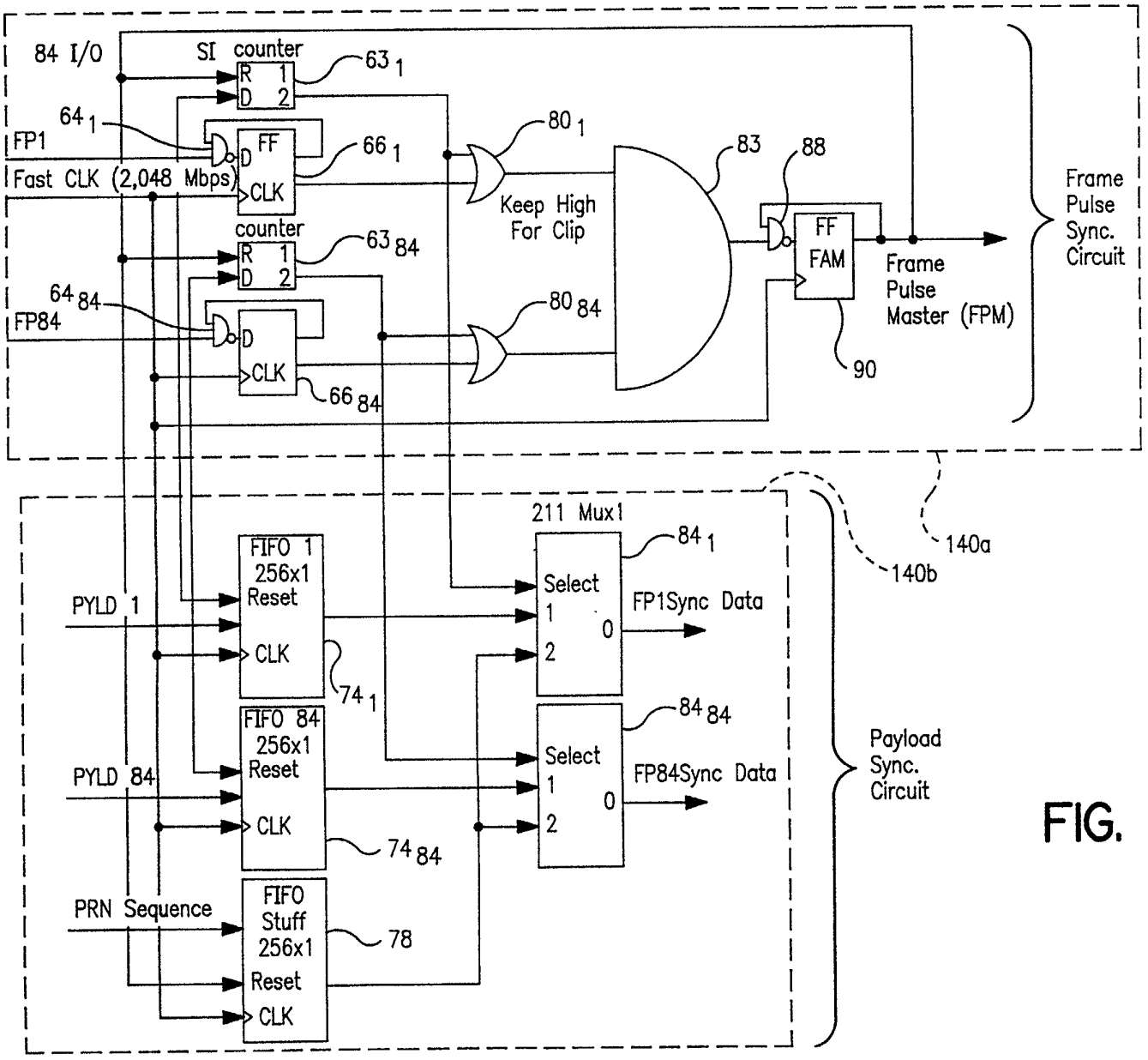
84 I/O
SI counter
R 1
D 2
63 1
64 1
FP1
FF
D
CLK
66 1
Fast CLK (2,048 Mbps)
80 1
Keep High For Clip
83
88
FF FAM
Frame Pulse Master (FPM)
Frame Pulse Sync. Circuit
90
counter
63 84
64 84
FP84
80 84
66 84
140a
140b
211 Mux1
FIFO 1 256x1 Reset
PYLD 1
CLK
74 1
Select
1
2
0
84 1
FP1Sync Data
FIFO 84 256x1 Reset
PYLD 84
74 84
84 84
FP84Sync Data
PRN Sequence
FIFO Stuff 256x1 Reset
78
Payload Sync. Circuit

FIG. 4

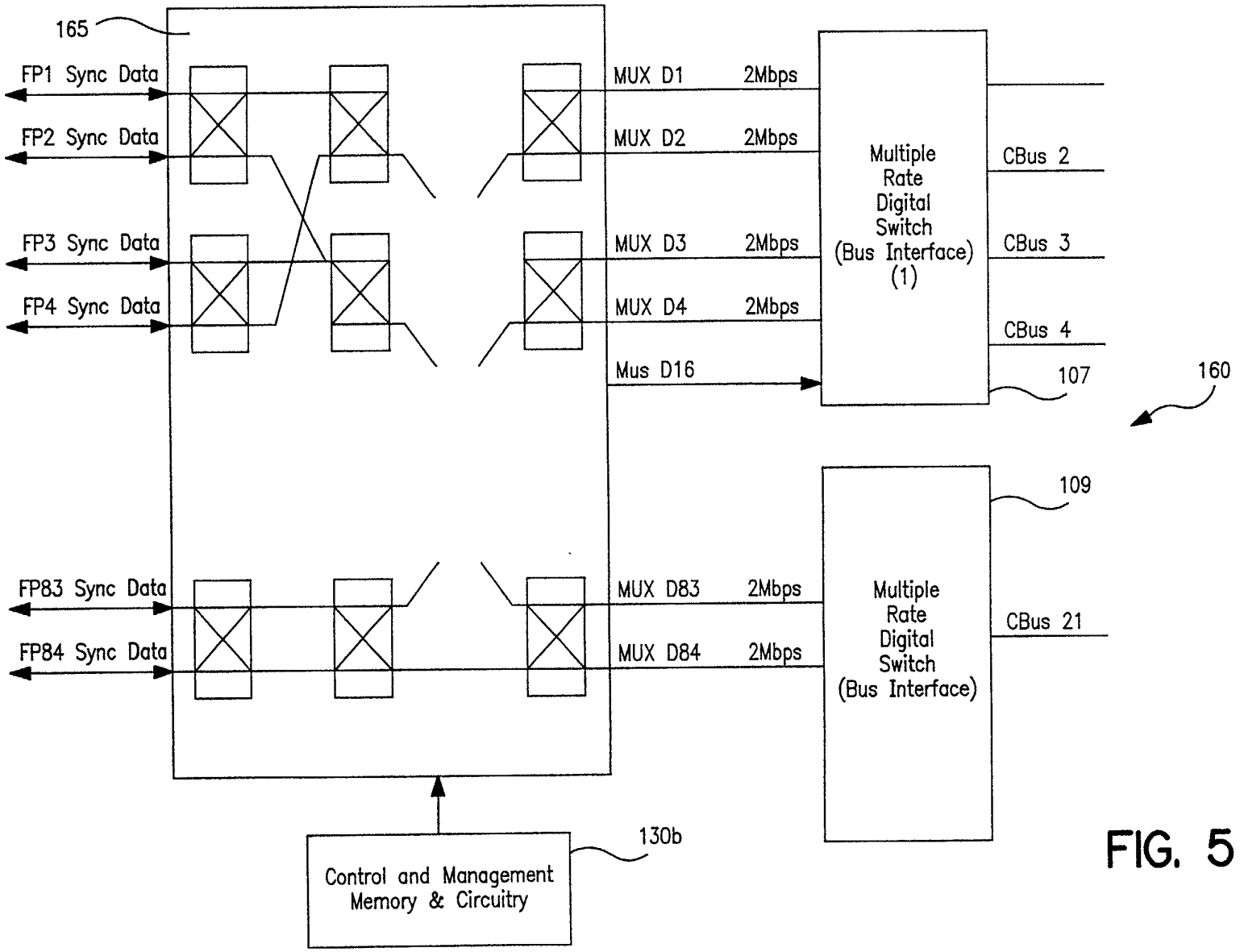
165
FP1 Sync Data
FP2 Sync Data
FP3 Sync Data
FP4 Sync Data
FP83 Sync Data
FP84 Sync Data
MUX D1 2Mbps
MUX D2 2Mbps
MUX D3 2Mbps
MUX D4 2Mbps
Mus D16
MUX D83 2Mbps
MUX D84 2Mbps
Multiple Rate Digital Switch (Bus Interface) (1)
CBus 2
CBus 3
CBus 4
107
160
109
Multiple Rate Digital Switch (Bus Interface)
CBus 21
130b
Control and Management Memory & Circuitry

FIG. 5

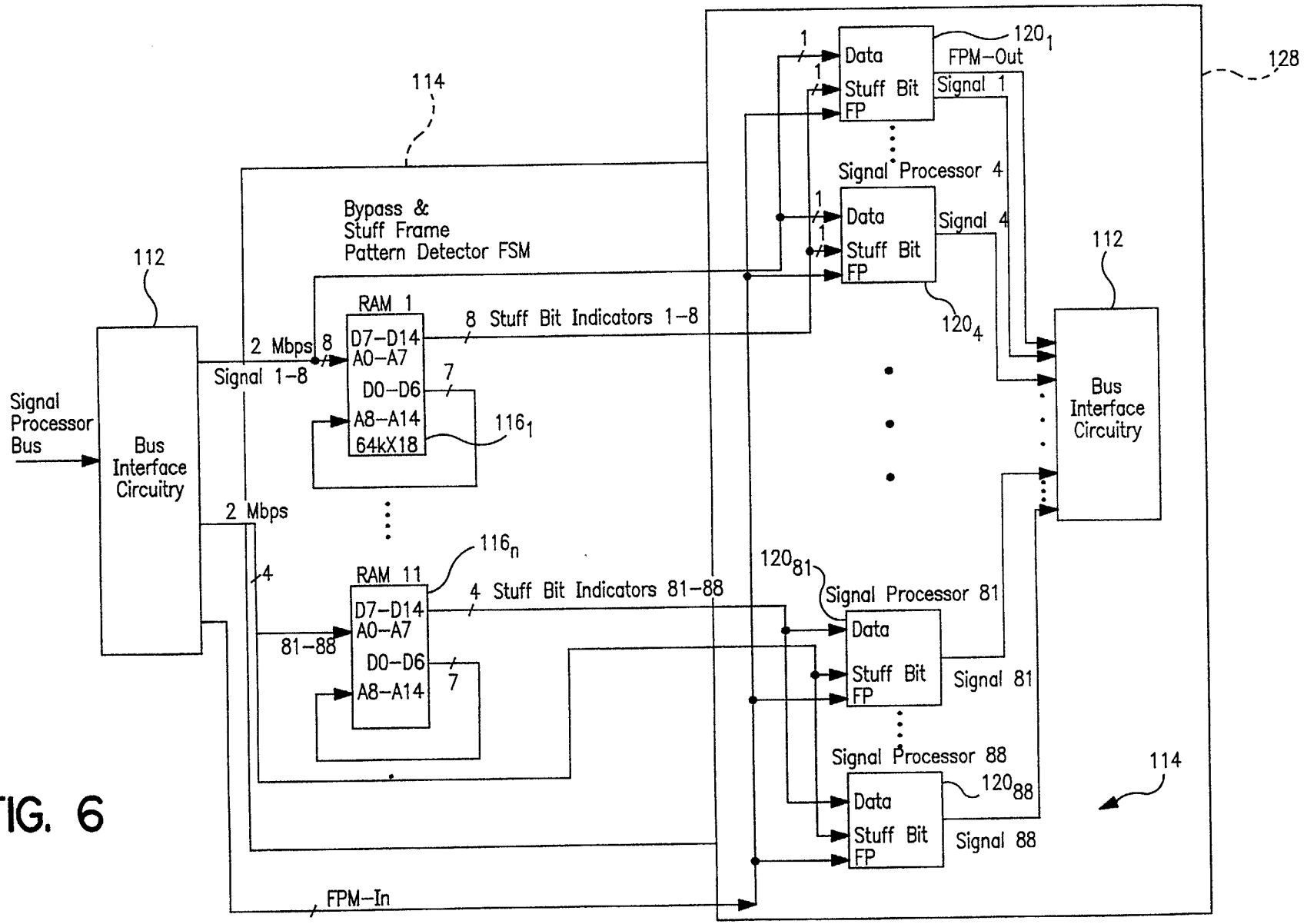

FIG. 6

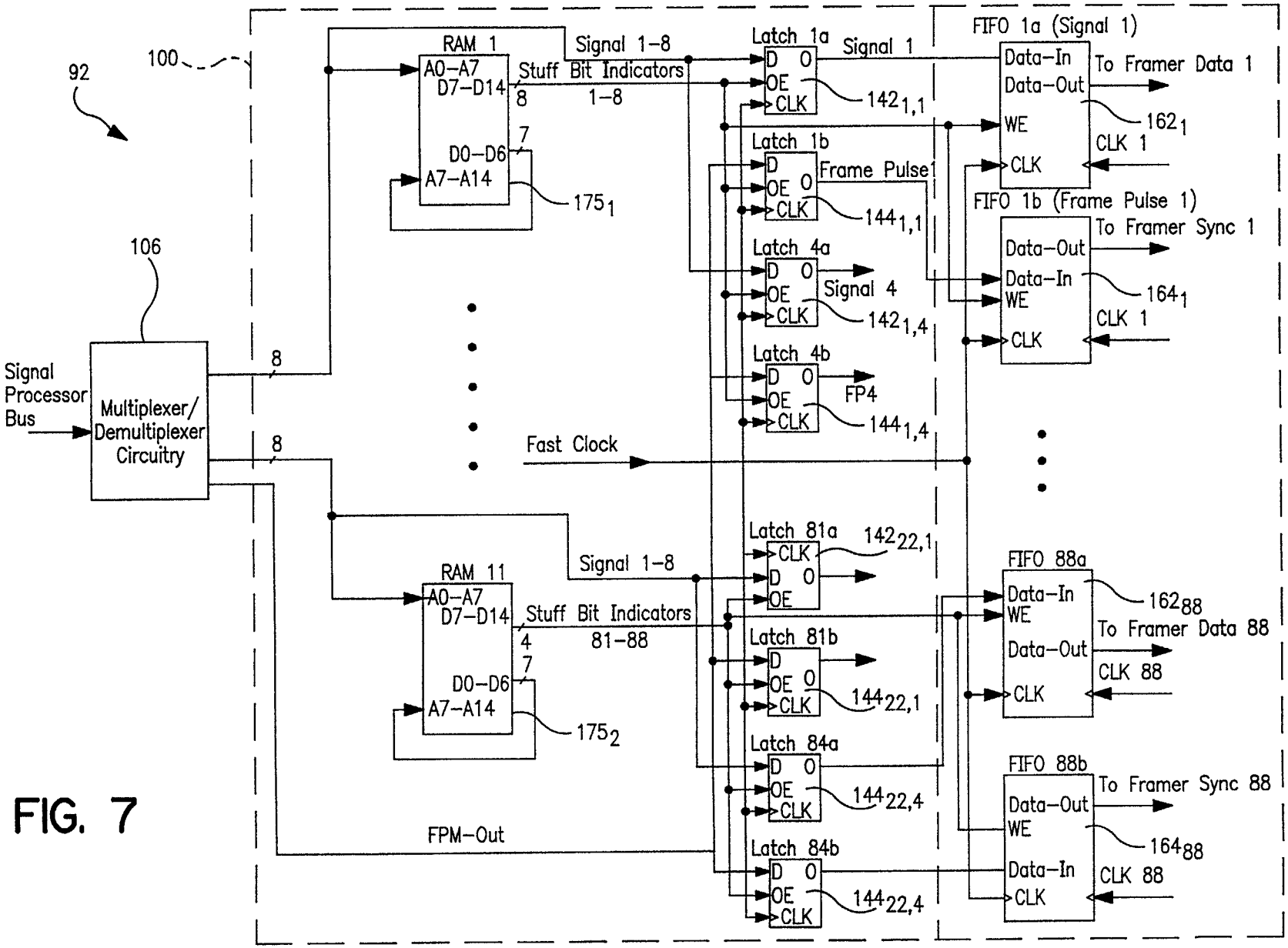
92
100
106
Signal Processor Bus
Multiplexer/ Demultiplexer Circuitry
8
8
RAM 1
A0–A7
D7–D14
8
D0–D6
A7–A14
7
175_1
Signal 1–8
Stuff Bit Indicators
1–8
RAM 11
A0–A7
D7–D14
4
D0–D6
A7–A14
7
175_2
Signal 1–8
Stuff Bit Indicators
81–88
Fast Clock
FPM–Out
Latch 1a
D
OE
CLK
Q
Signal 1
$142_{1,1}$
Latch 1b
Frame Pulse 1
$144_{1,1}$
Latch 4a
Signal 4
$142_{1,4}$
Latch 4b
FP4
$144_{1,4}$
Latch 81a
$142_{22,1}$
Latch 81b
$144_{22,1}$
Latch 84a
$144_{22,4}$
Latch 84b
$144_{22,4}$
FIFO 1a (Signal 1)
Data–In
Data–Out
WE
CLK
To Framer Data 1
162_1
CLK 1
FIFO 1b (Frame Pulse 1)
To Framer Sync 1
164_1
CLK 1
FIFO 88a
162_{88}
To Framer Data 88
CLK 88
FIFO 88b
To Framer Sync 88
164_{88}
CLK 88

FIG. 7